Operational Study of a Frequency Converter with a Control Sequence, Utilizing Xilinx Software

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Abstract: The paper analyses the operation of a single phase – three phase frequency converter, built with insulated-gate bipolar transistors (IGBT). The bridge inverter control is made via the Basys 2 development board which generates voltages, at the output terminals, compatible with the logic levels of complementary metal–oxide–semiconductor (CMOS) circuits. The diagram for obtaining the control pulses is realized with Xilinx software that allows changing the output frequency to a value of 1 KHz. The analysis of converter operation shall be made using either a resistive load or an inductive load. The installation model presented in the paper highlights the operation modality and the study possibility, by experiments at various frequencies and load circuits. By analyzing the waveforms obtained in various points of the circuit diagram, it results the possibility to improve certain operating parameters over others, according to the user requirements and the regulations in force for a harmonic regime.

Keywords: frequency converter; galvanic separation circuit; pulse sequence; development board; circuit switching; DC/AC power convertors

1 Introduction

Static power converters include complex techniques including circuit switching, control, regulation and conversion, using power semiconductors, diodes, transistors, etc., completed by auxiliary measurement and protection circuits. A spectacular evolution in the conversion of electrical energy was produced by the development and emergence of new power semiconductor devices which facilitated the improvement and diversification of the power converter, which is the element situated between the power supply and the power consumer. The purpose of this element is to convert the shape and parameters of electrical energy according to customer requirements, conversion characterized by high efficiency and reduced generation of high-order harmonics in power networks or to the power consumer. [8]

Most of the current technological processes of the various industrial sectors, increasingly require cheap, but robust electric motors. The DC motors with an adjustable speed have limited the scope of use due to the presence of brushes and mechanical collectors, which reduce operational reliability and is a risk factor, due to the sparks that can occur in presence of a flammable (explosive) environment. Therefore, it became imperative to develop drive systems with motors without sliding contacts, which have at least the adjustment performances in dynamic regime by the previous DC motors.

It should be noted the progress made by the emergence of digital signal processors (DSP), which, thanks to their greatly increased computing power (i.e. multiplication and addition in one cycle, clock rates of hundreds of MHz), enable the real-time implementation of complex and sophisticated algorithms.

The rapid growth of technology development and the progress in the field of power electronics, now allow for the development of extremely efficient electric drive equipment. The commensurate development of microelectronics and information technology has resulted in major changes within the field of electronic machine control, and the emergence of digital signal processors dedicated to digital motion control make possible the widespread deployment of control numerical algorithms. An important benefit for electric drives is shown in the development of intelligent power modules, incorporating either control or protection devices. Given the currently evolving direction of the high performance electric drives, it is obvious that large-scale development of numerical control algorithms plays an extremely important role.

The reconfigurable circuit board (FPGA), offers a compromise between the performances of a specific circuit and the flexibility of a software programmable circuit. These circuits are characterized by their ability to implement specialized circuits directly in the hardware. In addition, they can be easily modified when the operating conditions and/or dataset changes. [3]

The digital circuits are easier to design and test, because they can be designed from the logic gate level or functional level. The FPGA circuits have one of the shortest development and market integration timeframes. The FPGA circuits are inherently reconfigurable circuits, this feature alone allows for greater flexibility.

2 The Control Circuit

The control sequence requires 6 pulse trains of alternating ones and zeroes, so as to obtain simultaneously, three signals on a 1 and the others on a 0, corresponding to the transistors needing to be controlled in the three-phase output voltage system. For this, we used the clock signal of the development board, whose frequency is reduced by a division circuit made in the VHDL code (Figure 1) [1].

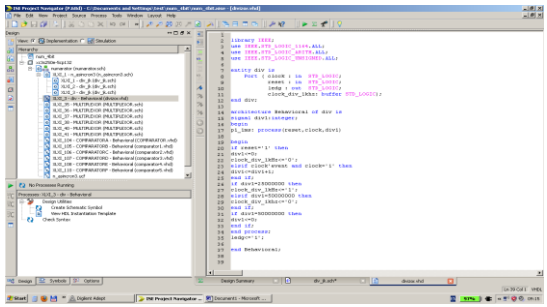


Figure 1

The VHDL code for the frequency divider

By means of the division circuit, we obtain the desired control frequency. From the division circuit we have also obtained the clock signal for the counter, comparators and multiplexers. The counter (Figure 2) is a three-bit asynchronous counter made with T-type flip-flops (Figure 3). For obtaining the 6 control sequences of the IGBT transistors, the counter was supplemented with a circuit for the identification of the 6th status (110), which then, initializes its status.

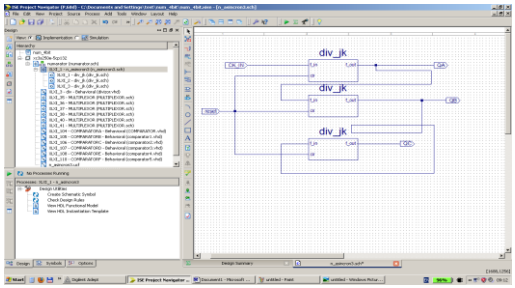


Figure 2

The 3-bit asynchronous counter realized in Xilinx

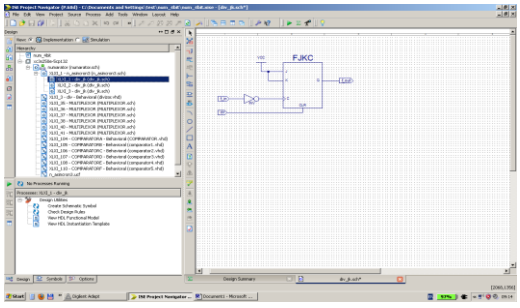


Figure 3

T-type flip-flop circuit

For each counter output sequence, the selection of each comparator is made via the control logic. We made six comparators in VHDL code, each comparator having entered in its structure the code corresponding to the IGBT transistors for 1/6 of the control sequence (Figure 4).

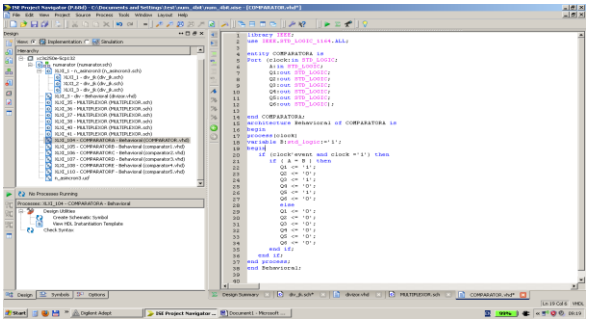


Figure 4
The VHDL code for a comparator

The comparator outputs are connected to the inputs of six multiplexers controlled by the counter output sequence (Figure 5). For each of the six control sequences, each multiplexer selects one of the counter output sequence. The multiplexer selection is made via a logical structure that receives commands from the counter output. Each of the six output states of the counter allows for the selection of a different sequence, corresponding to the control requirement of the bridge inverter transistors. The multiplexer outputs are brought via the output pins of the Basys2 board to the galvanic separation circuit for the transistor inverter controls.

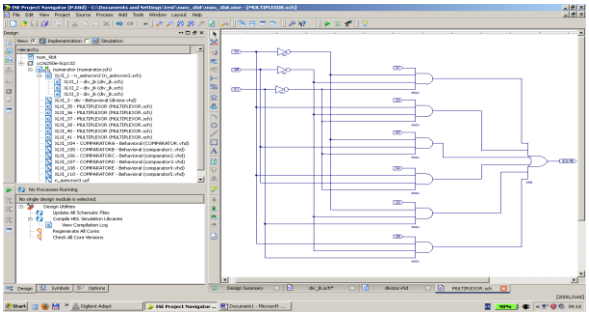


Figure 5
The multiplexer realized in Xilinx

For obtaining the control signals with "dead time" between the transistor control sequences we use a second divider, whose frequency is 10 times higher than the frequency of the first divider. This signal is used as a clock pulse for the second modulo-10 counter. The signals from the counter output go through an OR gate with 4 inputs which controls 6 AND gate circuits with two inputs and to the other

input of each AND gate arrive the signals from the multiplexer outputs (Fig. 6). Thus, at the output we obtain a control sequence for each transistor with a pause time 10 times lower than the normal clock sequence.

From the above, we can obtain the complete diagram (Figure 6) which allows obtaining the control sequence (Figure 7) at the output connectors of the board. [2]

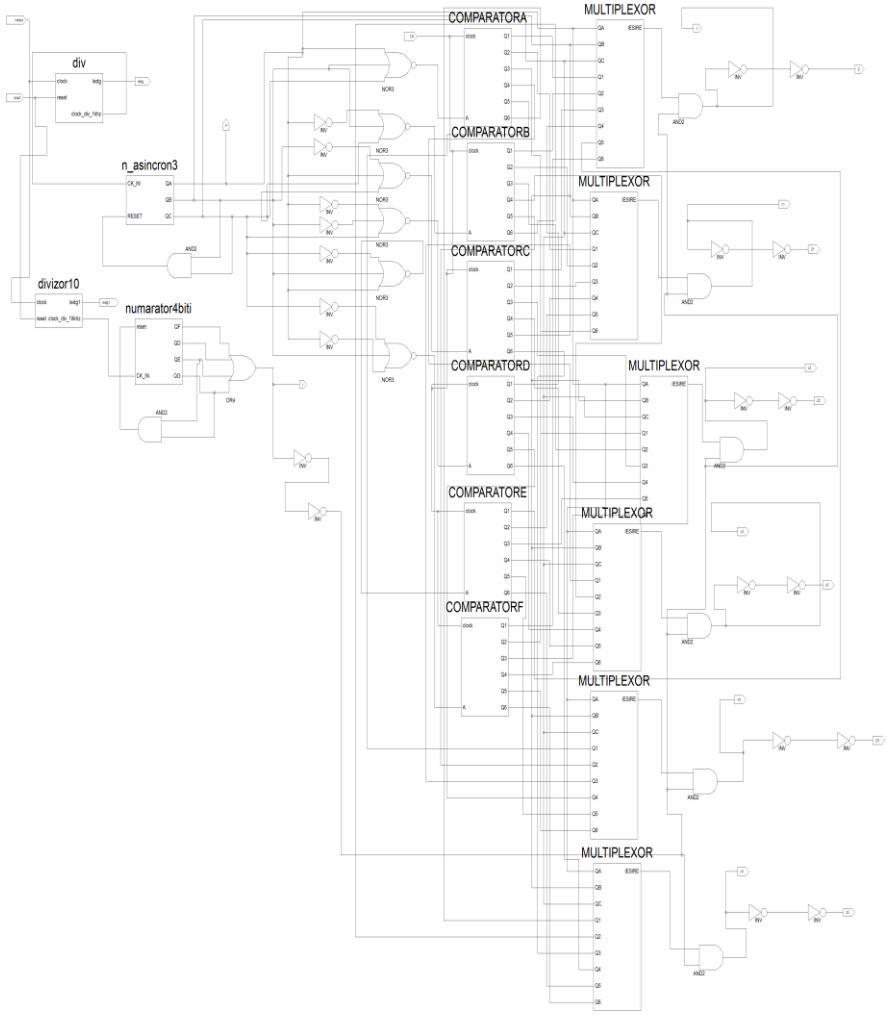


Figure 6
The control circuit diagram for obtaining the control sequences realized in Xilinx

3 Results and Discussions

We can see (Figure 7) the six control sequences corresponding to the transistors of the bridge inverter, either in graphic form, or as number sequence. [3]

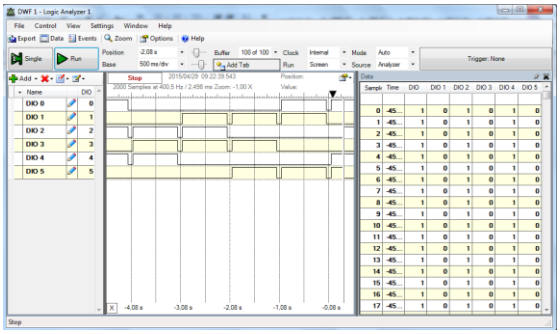


Figure 7
Inverter control sequence

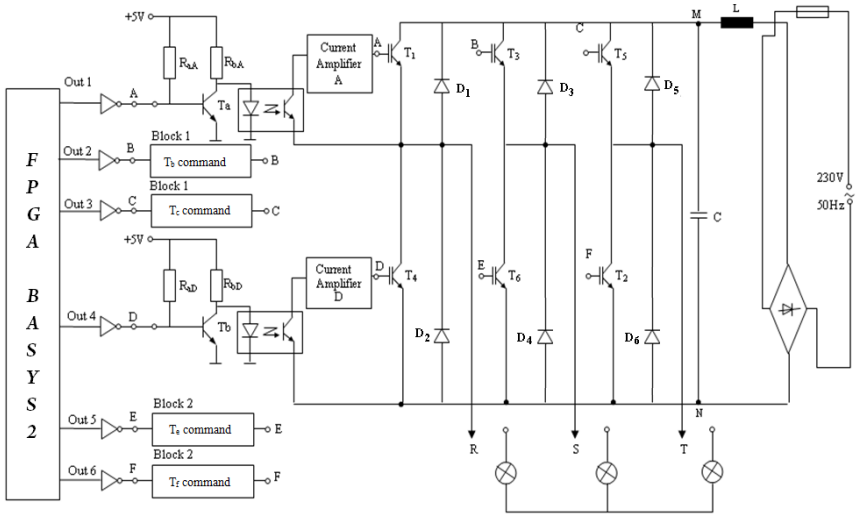


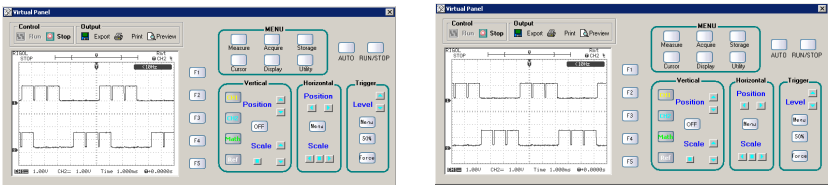
Figure 8
The diagram of the transistor voltage inverter – IGBT

The converter diagram (Figure 8) contains a galvanic separation circuit, a control pulse amplifying circuit, a single phase rectifier circuit, an intermediate DC circuit and the transistor bridge inverter IGBT. [4], [5], [6]

The control sequence of the Basys2 board is brought via MOS inverters and power amplifiers at the input of six optocouplers. They control, via the amplifier circuits, the transistor gates of the bridge inverter. [11]

The control sequence is obtained from the clock counter and is formed of six intervals, the resulting frequency being six times lower than the clock frequency.

From the pins of the Basys2 board connector, via a MOS inverter, the control signal is brought amplified in current by the transistors Ta…Tf at the inputs of the six optocouplers [1]. Examples are presented for three pairs of such sequences, i.e.: UCE voltage for Ta, UCE voltage for Tb (Figure 9a), UCE voltage for Ta, UCE voltage for Td (Figure 9b), corresponding to the frequency of 166.66 Hz, value obtained from the 1 KHz clock frequency of the counter divided by six, the circuit having a resistive load connected to the output.



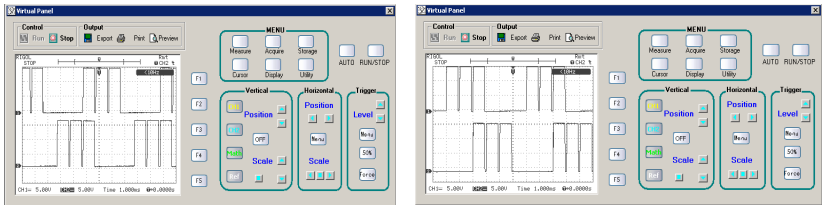
(a) (b)

Figure 9

Control voltages at optocouplers in the collector terminal of the transistors Ta and Tb (a) and Ta and Td (b)

By analyzing the waveforms obtained using the digital oscilloscope and stored on a PC, it appears to be a delay in the control sequence specific to the transistor pairs.

The control sequences in the collector terminals of the transistors Ta…Te are galvanicaly separated using optocouplers, and amplified in current with six amplifiers, each one provided with a high power switching transistor. The amplifier output is brought to the transistor gates of the bridge inverters. We present the emitter gate voltages for the transistors T4 and T6 (Figure 10a), T4 and T2 (Figure 10b).



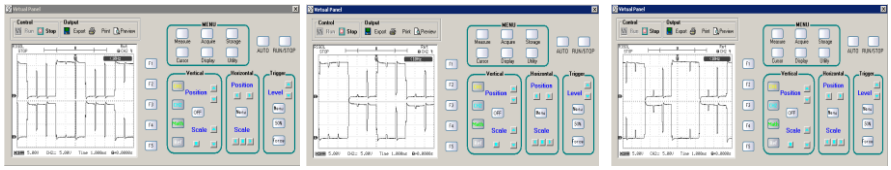
(a) (b)

Figure 10

The emitter gate voltage for the transistors T4 and T6 (a) and T4 and T2 (b)

We further present the waveforms for the emitter gate voltages for each of the three transistor pairs of the bridge inverter that has a resistive load connected as consumer. The visualization of the voltage pairs was made with a two-channel

digital oscilloscope which enables the data transfer into a computer system, as follows: the collector-emitter voltage U_{CE} for T_1 and T_4 (Figure 11a), U_{CE} for T_3 and T_6 (Figure 11b), U_{CE} for T_2 and T_5 (Figure 11c).

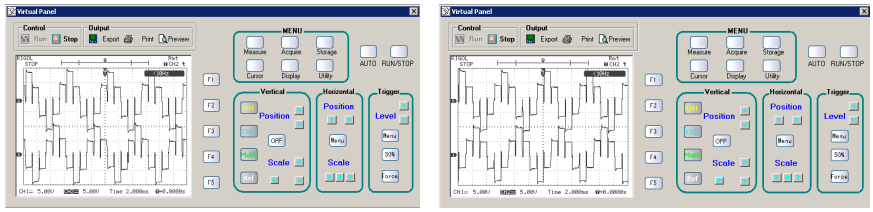


(a) (b) (c)

Figure 11

The collector-emitter voltage for the transistors T1 and T4 (a), for the transistors T3 and T6 (b) and for the transistors T5 and T2 (c)

From the analysis of the waveforms corresponding to the collector - emitter voltages of the transistor pairs of the bridge inverter at the frequency of 166 Hz, we obtain a complementary operation without switching delay or accidental switching. Further, we present the waveforms for the output voltages at the resistive load, as follows: the output voltages for the phases R and S (Figure 16), and the output voltages for the phases R and T (Figure 17). It can be seen that the output voltages have synthetic shape, with the phase angle shift of 120^o and without random switching.



(a) (b)

Figure 12

The output voltages: Phases R and S (a) and Phases R and T (b)

We present the emitter gate voltages and the emitter collector voltages for the transistors IGBT, at the clock frequency of 5 KHz, and the output voltages at the same frequency, the converter being connected to the same resistive load (Figure 13). [11]

In accordance with the commands at 833 Hz, we represent the emitter collector voltages for the transistors T1 and T4 (Figure 14), being the same for the other pairs of transistors T3-T6 and T5-T2, the reason why they will not, will be shown in separate figures.

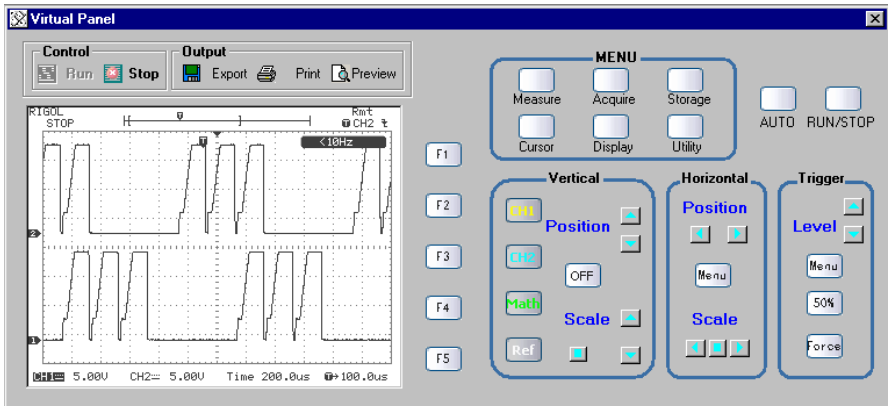


Figure 13
The GE voltages for the transistors T4 and T6 at 833 Hz

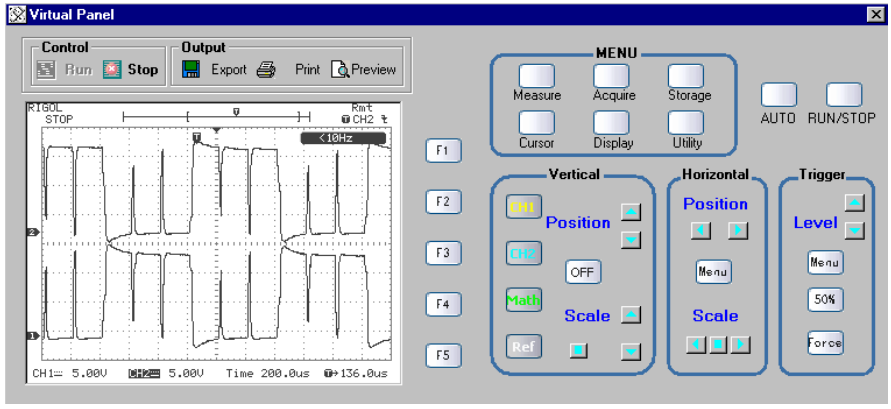
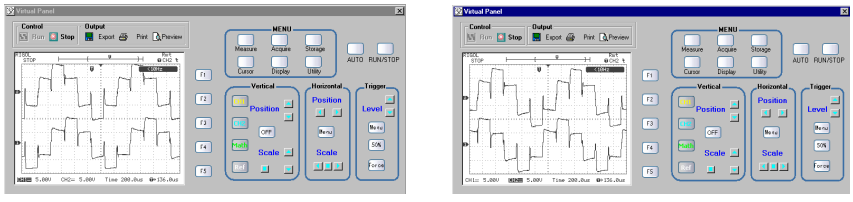


Figure 14
The UCE voltages for the transistors T1 and T4

The proper operation of the inverter at resistive load is evidenced by the waveforms of the output voltages U_{RS} and U_{RT}.



(a) (b)

Figure 15
The output voltages: Phases R and S (a) and Phases R and T (b)

The inverter operation was also checked with inductive load; more precisely, we controlled a 0.37 kW three-phase asynchronous motor with squirrel cage rotor. [7], [9]

The waveforms for the output voltages U_R and U_S at inductive load are visualized on an analogue oscilloscope at the clock frequency of 1 KHz, which corresponds to the motor control frequency of 166.6 Hz (Figure 16), and to the clock frequency of 2 KHz, which corresponds to the motor control frequency of 333.3 Hz (Figure 17).

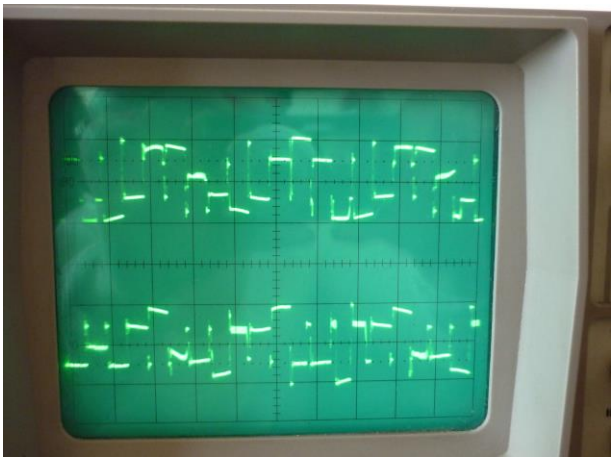


Figure 16
The U_R and U_S voltages

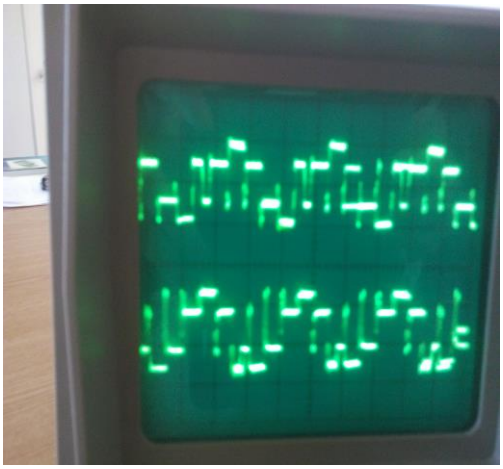


Figure 17
The output voltages - Phases U_R and U_S

There is deterioration in the operation of the bridge inverter transistors, particularly, during their blocking, when there is a relatively small exponential variance, but which does not affect the output voltage so profoundly. This can be seen in Figure 18. [10]

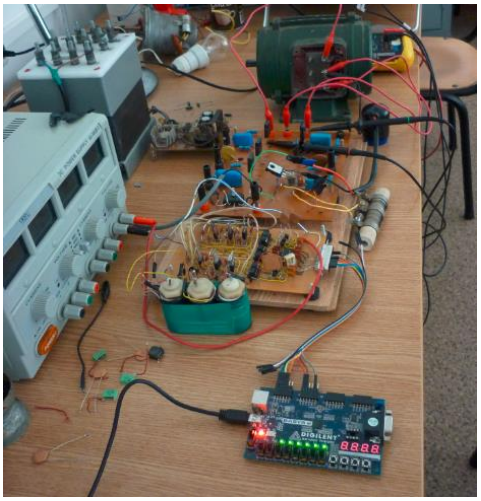


Figure 18
The model made to study the frequency converter

Conclusions

Herein it was found that the frequency converter operates properly. The converter is designed to operate with full wave control signal and being only laboratory equipment, was operated with a low load. The correct operation of the converter components is shown through the waveforms at certain points within the circuit. The operation analysis was carried out at resistive load, up to the frequency of 833 Hz and at inductive load at a frequency of 333.3 Hz. These values resulted by dividing the clock frequencies of 5 KHz and 2 KHz by 6, a number representing the control sequences of the inverting bridge. The measurements for the resistive load were made with a digital oscilloscope and those for the inductive load were made with an analog oscilloscope. The converter output frequency can be increased to greater than 800 Hz, but verification can be made only on the resistive load, because certain problems usually occur with the inductive load at frequencies above 400 Hz (iron loss and overheating of the bearings).

The installation model presented in this work (Figure 18) highlights the operational modality and the study possibilities by experimentation at various frequencies and load circuits.

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