Combinatorics at Electronic Circuit Realization in FPAA

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Abstract: Our present work is to examine and offer an automatic electronic circuit construction solution which – using electronic devices and Field Programmable Analog Arrays (FPAA) – enables us to form analogue circuits. The automatic computer-assisted construction is an old endeavor in the electronic development of electronic circuit constructional tasks. The currently used constructional systems are integrated devices which contain simulation modules based on circuit drawings and component parameters. It is relevant in printed circuit construction as well, where wiring geometry can be modified depending on the examined (EMC, thermo-technical, transmission\ldots, etc.) parameters. To achieve this goal, new simulation and circuit generation processes are required, which select the most appropriate solutions regarding the parametrical description of electronic topology.

1 Introduction

The two basic steps of analog electronic circuit construction are the provision of topology and their of the component parameters. Besides most extensive computer assistance, necessaries heuristic approaches in circuit arrangement. As a result of our development the prototypical circuit and its parametrical examination can result in the modification of the component parameters and the change of the topology. This process – reducing the number of iterations – can be accelerated if circuit simulation programs are applied. We reveal a process using of informatics resources facilitates the automatization of the construction [3] [6] [5] [4].

1.1 Circuit Description, Construction

The electronic circuit the connection matrices (K_c) are used for a network's description widespread in a simulation. The network according to the Figure 1 it a matrix writes it down Equation (1). This matrix has information about the connec-

tion between the nodes and its direction. The columns of the matrix contain the branches beginning there end from the single node while the rows write the single branches being attached to junctions down [2].

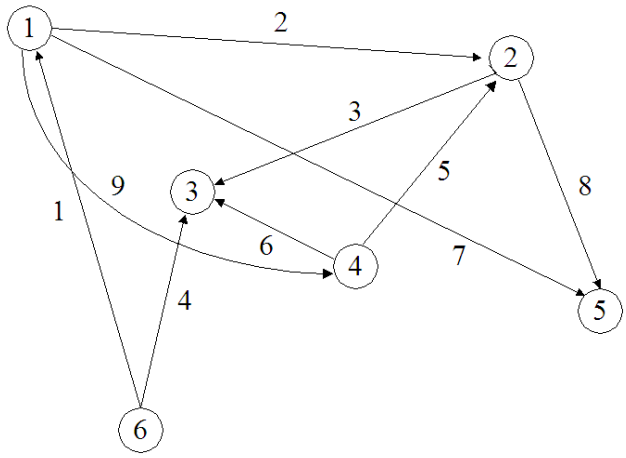


Figure 1
Graph and nodes of an electronic circuit

Likewise the cited from literature we know that it is a Figure 1 and for its graph and its branches an electronic component writes the relation of current down in Equation (1). The computerized electronic circuit simulation means the calculation of voltages to the single branch of the graph. Widespread procedures which can be applied well stand onto a provision in this direction.

$$\begin{array}{c} \\ b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \\ b_7 \\ b_8 \\ b_9 \end{array} \begin{array}{c} \begin{array}{cccccc} n_1 & n_2 & n_3 & n_4 & n_5 & n_6 \end{array} \\ \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \end{array} = \mathbb{K}_c \qquad (1)$$

The electronic circuit left to the computer totally construction in this manner, the single branches of the Figure 1 for his function draw, then these means his draw to his linking.

A random generated electronic circuit differing with a given parameters the simulation results of the transfer of an amplitude frequency of the Figures 2, on below visible of the properly circuit and its frequency-transfer [11] [12] [13] [17] [18].

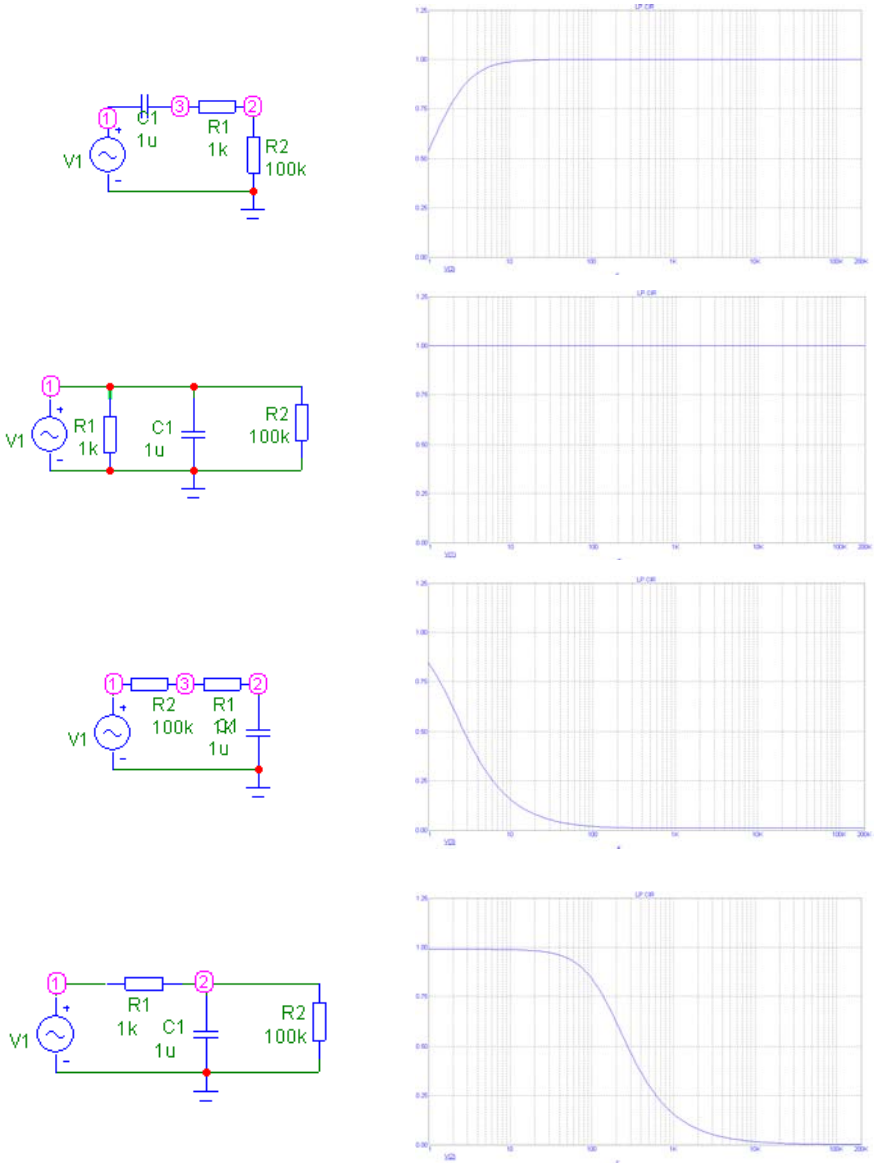


Figure 2

Any of the random circuits (left) the voted circuits (right) their frequency transfers

2 Circuit Definition in FPAA by Combinatoric Vote

The number of functional units in a particular FPAA device (Figure 3) is limited, since each of the four CABs has a limited elemental circuit. The number of inputs and outputs of FPAA is expected to be set. The various connect condition of I puts and outputs also narrows the number of possibilities due to the general rule of connecting the functional units.

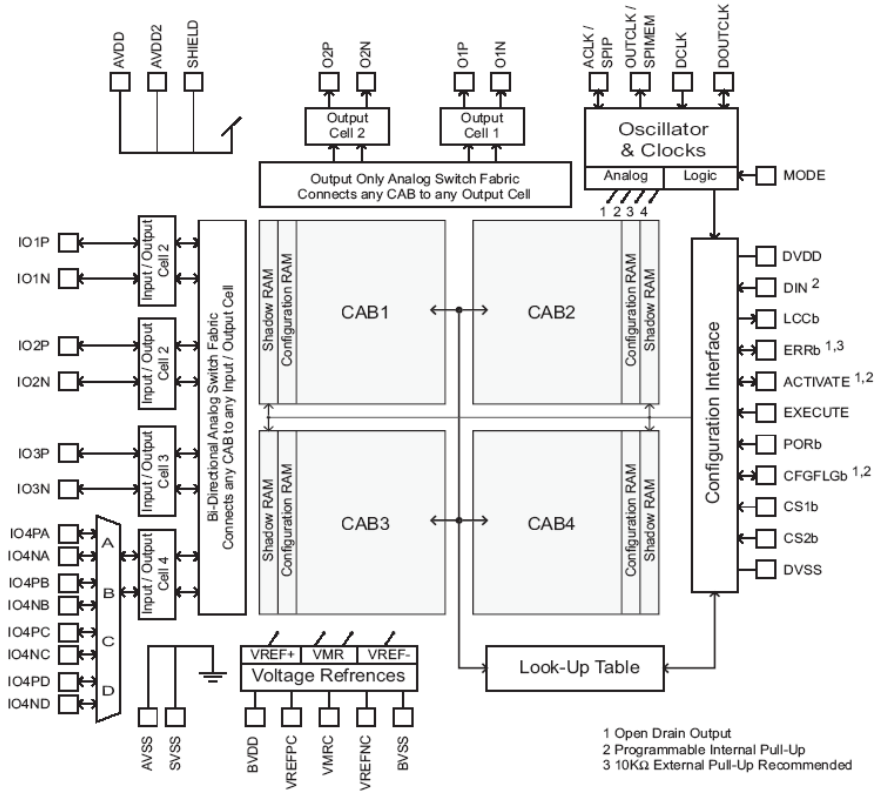


Figure 3
Inner structure of Anadigm's FPAA circuit

Figure 5 shows the list of the functional blocks. Weighing indicates the complexity of the particular blocks. '*A*' stands for the operational amplifiers, '*C*' for the condensers. Thus, we can form as many functional units in a CAB which require not more than three operational amplifiers and four condensers. As the Figure 3 shows in one CAB only one peak detector (CS) and two inverter differentiator amplifiers (DI) can be configured.

Figure 4 describes the simplified model of a potential operation amplifier in one of the branches. The model, in this case, describes the relation between branch voltages and branch circuits [13] [17].

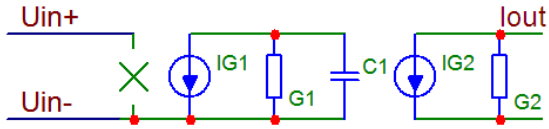


Figure 4
Equivalent circuit of operating amplifier

FPAA (AN221E04) mentioned in the introduction programmable like that electronic circuit, in which the electronic circuit details which can be developed with electronic circuit macros can be realized. These his quality and his quantity automatically the used depends of FPAA. On Figure 5 in Anadigm FPAA circuit macros visible.

The Kirchhoff-equation 4, deciding of the constructed circuit. The equation it was thawing out on Figure 5 from the possible CAMs different combinations which can be developed writes it down [10] [14] [1].

The Equation (3) pays attention to the quantity of the CAMs which can be worked up bar, the figure right being table based on the column of *Weight* as follows

$$q = \begin{pmatrix} r_{CAM} \\ m_s \end{pmatrix} \tag{2}$$

and

$$r_{CAM} = \sum_{\substack{0<A\le 3 \\ 0<C\le 8}} r_{CLB}\ (A, C), \tag{3}$$

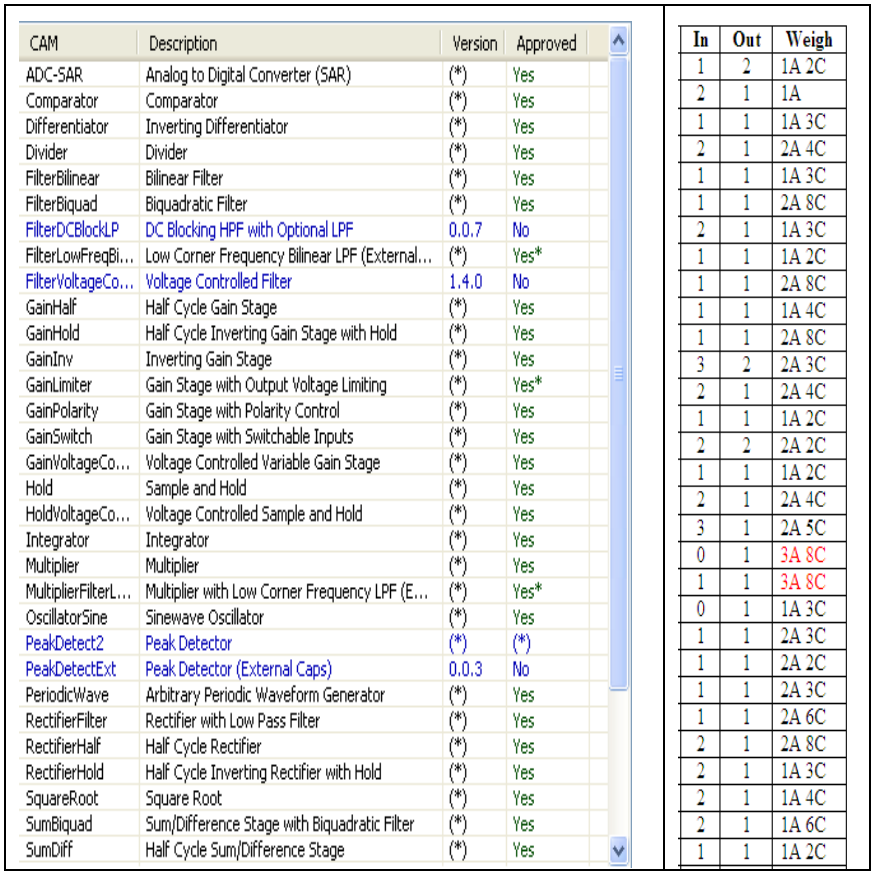
where A is the used amplifiers in CAMs, C is the used capacitors in CAMs.

The Equation (4), and (5) give the number of the possible connections.

The value of q decides the Equation (4)

$$q' = \left. \frac{m_s!}{r_{CAM}(m_s - r_{CAM})!} \right|_{\substack{0<A\le 3 \\ 0<C\le 8}} \tag{4}$$

where q is the number of abilities functional circuit (Configurable analog modules, CAM) in FPAA, m_S is the number of abilities different CAM in FPAA, r_{CAB} is the number of permissible CAMs.



CAM	Description	Version	Approved
ADC-SAR	Analog to Digital Converter (SAR)	(*)	Yes
Comparator	Comparator	(*)	Yes
Differentiator	Inverting Differentiator	(*)	Yes
Divider	Divider	(*)	Yes
FilterBilinear	Bilinear Filter	(*)	Yes
FilterBiquad	Biquadratic Filter	(*)	Yes
FilterDCBlockLP	DC Blocking HPF with Optional LPF	0.0.7	No
FilterLowFreqBi...	Low Corner Frequency Bilinear LPF (External...	(*)	Yes*
FilterVoltageCo...	Voltage Controlled Filter	1.4.0	No
GainHalf	Half Cycle Gain Stage	(*)	Yes
GainHold	Half Cycle Inverting Gain Stage with Hold	(*)	Yes
GainInv	Inverting Gain Stage	(*)	Yes
GainLimiter	Gain Stage with Output Voltage Limiting	(*)	Yes*
GainPolarity	Gain Stage with Polarity Control	(*)	Yes
GainSwitch	Gain Stage with Switchable Inputs	(*)	Yes
GainVoltageCo...	Voltage Controlled Variable Gain Stage	(*)	Yes
Hold	Sample and Hold	(*)	Yes
HoldVoltageCo...	Voltage Controlled Sample and Hold	(*)	Yes
Integrator	Integrator	(*)	Yes
Multiplier	Multiplier	(*)	Yes
MultiplierFilterL...	Multiplier with Low Corner Frequency LPF (E...	(*)	Yes*
OscillatorSine	Sinewave Oscillator	(*)	Yes
PeakDetect2	Peak Detector	(*)	(*)
PeakDetectExt	Peak Detector (External Caps)	0.0.3	No
PeriodicWave	Arbitrary Periodic Waveform Generator	(*)	Yes
RectifierFilter	Rectifier with Low Pass Filter	(*)	Yes
RectifierHalf	Half Cycle Rectifier	(*)	Yes
RectifierHold	Half Cycle Inverting Rectifier with Hold	(*)	Yes
SquareRoot	Square Root	(*)	Yes
SumBiquad	Sum/Difference Stage with Biquadratic Filter	(*)	Yes
SumDiff	Half Cycle Sum/Difference Stage	(*)	Yes

In	Out	Weigh
1	2	1A 2C
2	1	1A
1	1	1A 3C
2	1	2A 4C
1	1	1A 3C
1	1	2A 8C
2	1	1A 3C
1	1	1A 2C
1	1	2A 8C
1	1	1A 4C
1	1	2A 8C
3	2	2A 3C
2	1	2A 4C
1	1	1A 2C
2	2	2A 2C
1	1	1A 2C
2	1	2A 4C
3	1	2A 5C
0	1	3A 8C
1	1	3A 8C
0	1	1A 3C
1	1	2A 3C
1	1	2A 2C
1	1	2A 3C
1	1	2A 6C
2	1	2A 8C
2	1	1A 3C
2	1	1A 4C
2	1	1A 6C
1	1	1A 2C

Figure 5

left; List of the ability FPAA's functional circuit and their properties (Anadigm), right; Number of inputs, and outputs of analog macros, and number in their used amplifiers and capacitors

The number of theoretical possibilities writes down the Equation (5)

$$t_{cir} = \left[2\binom{n}{2} \right]^{b}, \tag{5}$$

$$t_{cir} = \left[n(n-1) \right]^{b}, \tag{6}$$

where n is the nodes of circuit, b is the used branches in circuit.

Onto a general, maximum case, the number of the branches thins out less, than that number of the nodes Equation (7) as below,

$$b = n - 1, \tag{7}$$

On the other hand, the number of the accesses of the raffled branch electronic circuits and the general who and access defines the number of the nodes Equation (8) in the next,

$$n = \left(\sum r_{CAM-in} + r_{CAM-out}\right) + 2, \tag{8}$$

where r_{CAM_jin} is the number of inputs of branch-circuits, r_{CAM_jout} is the number of outputs of branch-circuits

$$s = t_{cir} q'. \tag{9}$$

In the Equation (9) s is the number of theoretical abilities of the voted circuits.

We may avail ourselves of similar conditions with additional limitations. The Figure 5 is the *Out* column of his table and his *In* column with in conformity with additional bindings in this manner [15] [16]. The Figure 6 the proposed electronic circuit generating process exemplifies it. As first step normalized component we make the calculations with parameters, in this manner the character of the function of the electronic circuit can be judged.

Let us make a choice as an example who the possible from 28 electronic circuits three in that manner, that let the conditions ($0<\Sigma A\leq 3$ and $0<\Sigma C\leq 8$) come true. So the Equation (4) gives 3276 different abilities circuit. Each of these electronic circuits are one input and one outputs and in FPAA there are two general inputs or outputs, so the Equation (8) gives n=8, and maximal number of branches from Equation (7) gives 7 value. It is the number of the possible connections in this manner according to the Equation (6) gives $1{,}72\cdot 10^{12.}$ In this manner from the equation 9 the possible full number of attempts will be $5{,}65\cdot 10^{15}$.

Conclusions

We emphasize that present paper contains a lot of hypothetic elements, our findings are not elaborated. However, the interim results are promising. Integrating the circuit description algorithm and the combinatorial processes, and also the simulation assisted decision procedure regarding the analogue circuit-construction process in FPAA circuits, can be considered as a novelty in our effort.

An implication for further research is to find circuit nonsense which would reduce the number of combinatorial possibilities and would be applicable for a particular FPAA type.

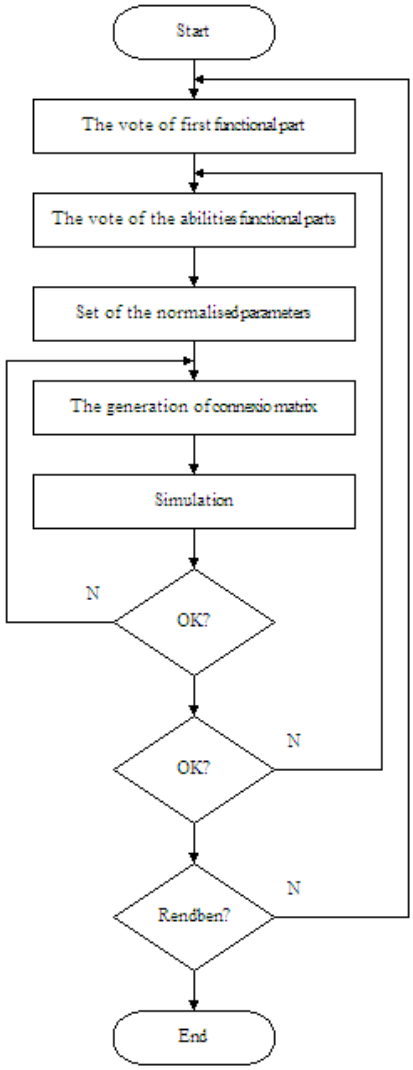


Figure 6
Flowchart of *brutal force* methods

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